

Exhibit 13

Part 2

Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

Nothing in Williams suggests that by manipulating features of this P+ doped region 317 (*e.g.*, forming an abrupt junction) one can impact the breakdown voltage of the device. Instead, to the extent Williams does attempt to address the breakdown voltage concern, it teaches providing "a protective diode cell 32" in the form of deep P+ diffusions that operate "to reduce the strength of the electric field across the gate oxide layers 306A, 306B and at the corners of the trenches and limits the formation of hot carriers in the vicinity of the trench." [Williams, col. 4, line 66 to col. 5, line 2]. This protective diode cell 32 "is provided for a selected number of MOSFET cells in a repetitive pattern across the MOSFET." [Williams, col. 5, lines 8-10]. Just as in Hshieh, this indicates that Williams also fails to appreciate the impact of an abrupt junction between a shallow heavy body junction and the well, and therefore does not contemplate such an abrupt junction even though it attempts to address a similar problem.

Thus, neither Hshieh nor Williams, nor the combination thereof, teaches or suggests, inherently or otherwise, a heavy body region that forms an abrupt junction with the well. Claims 46-96 are therefore patentably distinguished from the cited references for at least this reason.

2. Claims 97-120: The combination of Hshieh and Williams fails to teach or suggest the claimed dopant profile for the heavy body

Claims 97-120 recite a heavy body having "a region of high dopant concentration near the junction with the doped well and a region of relatively low dopant concentration near the surface of the substrate." As discussed above under VII.A.5, Hshieh does not disclose the claimed dopant profile in any of its junctions. Williams does not cure this deficiency. The Examiner has not pointed to any disclosure in Williams (or Hshieh) that is relevant to this element of the claims. Nor can the Appellants find any reference to a specific dopant profile for a heavy body region in either Hshieh or Williams. The combination of Hshieh and Williams therefore fails to teach or suggest such dopant profile. Claims 97-120 are thus patentably distinguished over the cited references.

3. Claims 65, 95 and 116: The combination of Hshieh and Williams fails to teach or suggest the claimed "distance between a bottom of the doped heavy body to the doped well junction"

As discussed above under VII.A.3, Hshieh fails to disclose a device wherein "a distance between a bottom of the doped heavy body to the doped well junction ranges from approximately 0.5 μm to 1.5 μm " as set forth in claims 65, 95 and 116. Williams does not cure this deficiency. Nowhere in Williams could the Appellants find any disclosure that would teach or even suggest the specific dimensions set forth in these claims. To the extent that the Examiner has argued, in connection with related claims 66 and 117, that dimensional limitations are *prima facie* obvious, Appellants submit that the dimensions recited in claims 65, 95 and 116 are for a particular unobvious purpose. As provided in the detailed description of the present application (e.g., page 6, lines 17-23), the inventors recognized that the depth of the heavy body junction relative to the well junction has an appreciable impact on electric fields in the active area. An advantage gained by designing a device with the relative dimensions as described in the application and set forth in the claims is the improvement in breakdown voltage.

Claims 65, 95 and 116 are therefore further patentably distinguished from the combination of Hshieh and Williams.

4. Claims 47, 69 and 98: The combination of Hshieh and Williams fails to disclose that the claimed "location of the abrupt junction...is adjusted"

Under section VII.A.6 above, Appellants discussed how Hshieh fails to teach, inherently or otherwise, that the "location of the abrupt junction relative to the well junction at the second depth is adjusted so that, when voltage is applied to the transistor, a peak electric field is spaced away from the trench in the semiconductor." Williams does not add anything in this regard. Again, to the extent Williams attempts to address the problem of destructive breakdown, it teaches providing "protective diode cells" repeated across the array of active cells. Nothing in Williams even suggests that the "location" of the junction between P+ region 317 and the underlying well 310 can influence the breakdown voltage of the device.

Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

Thus, the combination of Hshieh and Williams fails to disclose or suggest the claimed location of the heavy body junction relative to the well junction. Accordingly, claims 47, 68 and 98 are further patentably distinguished from the combination of the cited art.

5. Claims 58, 59, 79, 109, and 110: The combination of Hshieh and Williams fails to teach or suggest the claimed termination structure

Under section VII.A.7 above, Appellants discussed how Hshieh fails to teach a termination structure comprising "a plurality of concentric trenches surrounding the transistor" which is recited in claims 58, 79 and 109. Williams does not cure this deficiency. No teaching or suggestion could be found any where in Williams regarding a termination structure having a plurality of concentric trenches. The combination of Hshieh and Williams therefore fails to disclose or suggest a termination structure with a plurality of concentric trenches as recited in claims 58, 79 and 109.

Claims 59 and 110 define a termination structure with a termination trench "wherein the termination trench extends to substantially the same depth as the transistor trench." In rejecting these claims, the Examiner asserts that Williams teaches in Fig. 3 "a deep well 316 that functions as termination region surrounding the device that has a depth extends [sic] to substantially the same depth as the transistor trench," and that it would have been obvious to combine this teaching with the termination structure of Hshieh. Appellants submit that this rejection is based on a misunderstanding of the nature of the device disclosed in Williams. Deep well 316 is simply not a termination structure.

Referring to Williams' description of Fig.3, Williams explains that deep P+ diffusion 316 is "a protective diode" that is "provided for a selected number of MOSFET cells in a repetitive pattern across the MOSFET." [Williams, col. 4, line 57 to col. 5, line 14]. Therefore, deep P+ diffusion is clearly not a termination structure since it does not surround and terminate the active area of the transistor. Neither Williams nor Hshieh, nor their combination teaches or suggests any specific depths for a trench termination structure. Claims 59 and 110 are therefore further patentably distinguished over the cited references.

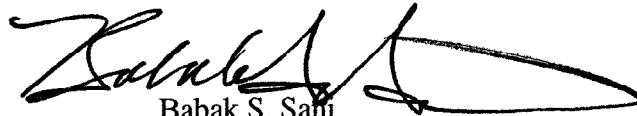
Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

CONCLUSION

In view of the foregoing remarks, Appellants respectfully request reversal of the rejections of all pending claims.

Respectfully submitted,



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Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

VIII. CLAIMS APPENDIX

46. (previously presented) A field effect transistor comprising:
a semiconductor substrate having dopants of a first conductivity type;
a trench extending a predetermined depth into the semiconductor substrate;
a doped well having dopants of a second conductivity type opposite to the first conductivity type and extending into the semiconductor substrate to form a well junction at a first depth;

a doped source region having dopants of the first conductivity type and extending into the semiconductor substrate to form a source junction at a second depth; and

a doped heavy body region having dopants of the second conductivity type and extending into the doped well to form a heavy body junction at a depth that is deeper than the source junction and shallower than the trench,

wherein the heavy body region forms an abrupt junction in the doped well.

47. (previously presented) The field effect transistor of claim 46 wherein a location of the abrupt junction relative to the well junction is adjusted so that, when voltage is applied to the transistor, a peak electric field is spaced away from the trench in the semiconductor.

48. (previously presented) The field effect transistor of claim 46 wherein the doped well has a substantially flat bottom.

49. (previously presented) The field effect transistor of claim 46 wherein the trench has rounded top corners.

50. (previously presented) The field effect transistor of claim 46 wherein the trench has rounded bottom corners.

51. (previously presented) The field effect transistor of claim 46 wherein the trench has rounded top and bottom corners.

Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

52. (previously presented) The field effect transistor of claim 46 wherein the heavy body comprises a heavily doped region formed by implanting dopants of the second conductivity type at an approximate location of the abrupt junction.

53. (previously presented) The field effect transistor of claim 46 wherein the trench is lined with a dielectric material and substantially filled with conductive material, wherein the conductive material substantially filling the trench is recessed relative to the surface of the substrate.

54. (previously presented) The field effect transistor of claim 46 wherein the substrate comprises a first highly doped region and a second doped region disposed above said first highly doped region, the second doped region having a lower doping concentration relative to the first highly doped region.

55. (previously presented) The field effect transistor of claim 54 further comprising a termination structure surrounding the transistor.

56. (previously presented) The field effect transistor of claim 55 wherein the termination structure comprises a doped region having dopants of the second conductivity type extending into the second doped region of the substrate to form a PN junction between the termination doped region and the second doped region of the substrate.

57. (previously presented) The field effect transistor of claim 55 wherein the termination structure comprises a trench.

58. (previously presented) The field effect transistor of claim 55 wherein the termination structure comprises a plurality of concentric trenches surrounding the transistor.

59. (previously presented) The field effect transistor of claim 57 wherein the termination trench extends to substantially the same depth as the transistor trench.

Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

60. (previously presented) The field effect transistor of claim 54 wherein the second doped region of the substrate has an initial thickness of less than $10\mu\text{m}$.

61. (previously presented) The field effect transistor of claim 54 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is less than $3\mu\text{m}$.

62. (previously presented) The field effect transistor of claim 54 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is approximately $1\mu\text{m}$.

63. (previously presented) The field effect transistor of claim 46 wherein the depth of the doped well ranges from approximately $1\mu\text{m}$ to $3\mu\text{m}$.

64. (previously presented) The field effect transistor of claim 46 wherein the depth of the doped heavy body ranges from approximately $0.4\mu\text{m}$ to $1.5\mu\text{m}$.

65. (previously presented) The field effect transistor of claim 46 wherein a distance between a bottom of the doped heavy body to the doped well junction ranges from approximately $0.5\mu\text{m}$ to $1.5\mu\text{m}$.

66. (previously presented) The field effect transistor of claim 46 wherein a distance between a bottom of the doped heavy body to the doped well junction is less than approximately $0.5\mu\text{m}$.

67. (previously presented) A field effect transistor comprising:
a semiconductor substrate having dopants of a first conductivity type;
a plurality of gate-forming trenches arranged substantially parallel to each other,
each trench extending to a first depth into said substrate, the space between adjacent trenches
defining a contact area;

Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

a doped well having dopants of a second conductivity type opposite to the first conductivity type and extending into the semiconductor substrate to form a well junction with the substrate;

a doped source region having dopants of the first conductivity type forming a source junction inside the doped well;

a heavy body having dopants of the second conductivity type and extending into the doped well to a second depth that is deeper than the source junction; and

heavy body contact regions defined at the surface of the semiconductor substrate along the length of the contact area,

wherein the heavy body forms an abrupt junction within the doped well.

68. (previously presented) The field effect transistor of claim 67, wherein said doped well has a substantially flat bottom.

69. (previously presented) The field effect transistor of claim 67 wherein a location of the abrupt junction relative to the well junction at the second depth is adjusted so that, when voltage is applied to the transistor, a peak electric field is spaced away from the plurality of gate-forming trenches.

70. (previously presented) The field effect transistor of claim 67 wherein said doped well has a depth less than the first depth of the gate-forming trenches.

71. (previously presented) The field effect transistor of claim 67 wherein each said gate-forming trench has rounded top corners.

72. (previously presented) The field effect transistor of claim 67 wherein each said gate-forming trench has rounded bottom corners.

73. (previously presented) The field effect transistor of claim 67 wherein each said gate-forming trench has rounded top and bottom corners.

Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

74. (previously presented) The field effect transistor of claim 67 further comprising a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a depth greater than the first depth of the plurality of gate-forming trenches.

75. (previously presented) The field effect transistor of claim 74 wherein the deep doped region forms a PN junction diode with the substrate.

76. (previously presented) The field effect transistor of claim 74 wherein the deep doped region forms a field termination structure surrounding the periphery of the plurality of gate-forming trenches.

77. (previously presented) The field effect transistor of claim 76 further comprising:

- a layer of dielectric material formed over the deep doped region; and
- a layer of conductive material formed on top of the layer of dielectric material.

78. (previously presented) The field effect transistor of claim 67 further comprising a field termination structure comprising a trench substantially surrounding the plurality of gate-forming trenches.

79. (previously presented) The field effect transistor of claim 78 wherein said field termination structure comprises a plurality of concentrically arranged trenches.

80. (previously presented) The field effect transistor of claim 67 wherein the heavy body forms a continuous doped region along substantially the entire length of said contact area.

81. (previously presented) The field effect transistor of claim 67 wherein said doped source region extends along the length of the trench.

Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

82. (previously presented) The field effect transistor of claim 81 further comprising a source contact region defined at the surface of the semiconductor substrate and configured to contact the doped source region.

83. (previously presented) The field effect transistor of claim 81 further comprising a plurality of source contact regions disposed along the length of the contact area in an alternating fashion with the plurality of heavy body contact regions.

84. (previously presented) The field effect transistor of claim 67 wherein between a pair of adjacent trenches a plurality of doped source regions are positioned on opposite sides of each trench, and wherein the heavy body is bounded by the pair of adjacent trenches and the doped source regions.

85. (previously presented) The field effect transistor of claim 67 wherein between a pair of adjacent trenches, the heavy body extends continuously parallel to the longitudinal axis of the trenches.

86. (previously presented) The field effect transistor of claim 67 further comprising:
a layer of dielectric material lining inside walls of each of said plurality of gate-forming trenches; and
a layer of conductive material substantially filling the gate-forming trenches.

87. (previously presented) The field effect transistor of claim 86 wherein the layer of conductive material comprises polysilicon.

88. (previously presented) The field effect transistor of claim 86 wherein the top surface of the layer of conductive material substantially filling the gate-forming trenches is recessed relative to the top surface of the semiconductor substrate.

Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

89. (previously presented) The field effect transistor of claim 67 wherein the substrate comprises a first highly doped region and a second doped region disposed above said first highly doped region, the second doped region having a lower doping concentration relative to the first highly doped region.

90. (previously presented) The field effect transistor of claim 89 wherein the second doped region of the substrate has an initial thickness of less than $10\mu\text{m}$.

91. (previously presented) The field effect transistor of claim 89 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is less than $3\mu\text{m}$.

92. (previously presented) The field effect transistor of claim 89 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is approximately $1\mu\text{m}$.

93. (previously presented) The field effect transistor of claim 67 wherein the depth of the doped well ranges from approximately $1\mu\text{m}$ to $3\mu\text{m}$.

94. (previously presented) The field effect transistor of claim 67 wherein the depth of the doped heavy body ranges from approximately $0.4\mu\text{m}$ to $1.5\mu\text{m}$.

95. (previously presented) The field effect transistor of claim 67 wherein a distance between a bottom of the doped heavy body to the doped well junction ranges from approximately $0.5\mu\text{m}$ to $1.5\mu\text{m}$.

96. (previously presented) The field effect transistor of claim 67 wherein a distance between a bottom of the doped heavy body to the doped well junction is less than approximately $0.5\mu\text{m}$.

Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

97. (previously presented) A field effect transistor comprising:
a semiconductor substrate having dopants of a first conductivity type;
a trench extending a predetermined depth into the semiconductor substrate;
a doped well having dopants of a second conductivity type opposite to the first conductivity type and extending into the semiconductor substrate to form a well junction at a first depth;
a doped source region having dopants of the first conductivity type and extending into the semiconductor substrate to form a source junction at a second depth; and
a doped heavy body region having dopants of the second conductivity type and extending into the doped well to form a heavy body junction at a depth that is deeper than the source junction and shallower than the trench, the doped heavy body region having a region of high dopant concentration near the junction with the doped well and a region of relatively low dopant concentration near the surface of the substrate.

98. (previously presented) The field effect transistor of claim 97 wherein a location of the heavy body junction relative to the well junction at the second depth is adjusted so that, when voltage is applied to the transistor, a peak electric field is spaced away from the trench in the semiconductor.

99. (previously presented) The field effect transistor of claim 97 wherein the doped well has a substantially flat bottom.

100. (previously presented) The field effect transistor of claim 97 wherein the trench has rounded top corners.

101. (previously presented) The field effect transistor of claim 97 wherein the trench has rounded bottom corners.

102. (previously presented) The field effect transistor of claim 97 wherein the trench has rounded top and bottom corners.

Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

103. (previously presented) The field effect transistor of claim 97 wherein the region of high dopant concentration in said doped heavy body region is formed by implanting dopants of the second conductivity type at an approximate location of the junction with the doped well.

104. (previously presented) The field effect transistor of claim 97 wherein the trench is lined with a dielectric material and substantially filled with conductive material, wherein the conductive material substantially filling the trench is recessed relative to the surface of the substrate.

105. (previously presented) The field effect transistor of claim 97 wherein the substrate comprises a first highly doped region and a second doped region disposed above said first highly doped region, the second doped region having a lower doping concentration relative to the first highly doped region.

106. (previously presented) The field effect transistor of claim 105 further comprising a termination structure surrounding the transistor.

107. (previously presented) The field effect transistor of claim 106 wherein the termination structure comprises a doped region having dopants of the second conductivity type extending into the second doped region of the substrate to form a PN junction between the termination doped region and the second doped region of the substrate.

108. (previously presented) The field effect transistor of claim 106 wherein the termination structure comprises a trench.

109. (previously presented) The field effect transistor of claim 106 wherein the termination structure comprises a plurality of concentric trenches surrounding the transistor.

110. (previously presented) The field effect transistor of claim 108 wherein the termination trench extends to substantially the same depth as the transistor trench.

Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

111. (previously presented) The field effect transistor of claim 105 wherein the second doped region of the substrate has an initial thickness of less than $10\mu\text{m}$.

112. (previously presented) The field effect transistor of claim 105 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is less than $3\mu\text{m}$.

113. (previously presented) The field effect transistor of claim 105 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is approximately $1\mu\text{m}$.

114. (previously presented) The field effect transistor of claim 97 wherein the depth of the doped well ranges from approximately $1\mu\text{m}$ to $3\mu\text{m}$.

115. (previously presented) The field effect transistor of claim 97 wherein the depth of the doped heavy body ranges from approximately $0.4\mu\text{m}$ to $1.5\mu\text{m}$.

116. (previously presented) The field effect transistor of claim 97 wherein a distance between a bottom of the doped heavy body to the doped well junction ranges from approximately $0.5\mu\text{m}$ to $1.5\mu\text{m}$.

117. (previously presented) The field effect transistor of claim 97 wherein a distance between a bottom of the doped heavy body to the doped well junction is less than approximately $0.5\mu\text{m}$.

118. (previously presented) The field effect transistor of claim 97 further comprising a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a depth below the trench.

119. (previously presented) The field effect transistor of claim 118 wherein said deep doped region forms a PN junction diode with the substrate.

Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

120. (previously presented) The field effect transistor of claim 119 wherein the deep doped region forms a termination structure.

Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

IX. EVIDENCE APPENDIX - NON-APPLICABLE

Appl. No. 10/630,249
November 3, 2005
Appeal Brief

PATENT

X. RELATED PROCEEDINGS APPENDIX - NON- APPLICABLE

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